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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,699	12/18/2001	Chi-Keung Luk	200302 184-1 (1662-46800)	3236

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EXAMINER	
TO, JENNIFER N	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,699	LUK ET AL.	
	Examiner	Art Unit	
	Jennifer N. To	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 are pending for examination.

2. Claims 8, 17, and 27 are objected because of the following minor error: duplicate of claims 7, 16, and 24.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory

double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1, 10, and 31 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, and 11 of U.S. Patent No. 6757811. Although the conflicting claims are not identical, they are not patentably distinct from each other because both computer systems comprise substantially the same elements. For example, claim 1 comprises the same elements claim 1 of U.S. Patent No. 6757811 (i.e. a processor capable of executing multiple threads vs. a pipelined simultaneously and redundantly thread (SRT) processor, a main system memory vs. a main system memory).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Dubey et al. (hereafter Dubey) (U.S. Patent No. 5812811).

9. As per claim 1, Dubey teaches the invention as claim including a computer system comprising:

a processor capable of executing multiple threads (col. 4, lines 50-53); and

a main system memory coupled to said processor (fig. 1A, item 100);

wherein said processor processes a program in a main thread that includes instructions which cause the processor to spawn a pre-execution thread in which only a portion, but not all, of the same program executes, said pre-execution thread runs concurrently with the main thread, but a head of the main thread in program order (abstract, lines 1-6; col. 4, lines 51-58; col. 6, lines 13-28; col. 7, lines 4-30; col. 8, lines 60-65; col. 15, line 45 through col. 16, line 13; col. 21, lines 25-38).

10. As per claim 2, Dubey teaches that wherein said instructions that cause the pre-execution thread to be spawn include a start instruction which causes a pre-execution thread to start and a stop instruction which causes the pre-execution thread to stop (col. 8, line 60 through col. 10, line 36).

11. As per claim 3, Dubey teaches that wherein said start instruction includes a value designating the location in the program where the pre-execution thread is to start running (col. 9, lines 50-67).

12. As per claim 4, Dubey teaches that wherein the pre-execution thread encounters a cache miss condition for a memory reference but the main thread does not encounter a cache miss condition when that same memory reference is processed by the main thread (col. 15, lines 5-40).

13. As per claim 5, Dubey teaches that wherein said processor determines whether sufficient hard ware resources are available before spawning said pre-execution thread (col. 15, lines 59-64; col. 29, lines 21-23).

14. As per claim 6, Dubey teaches that wherein said processor ignores exception conditions generated during the pre-execution thread (col. 16, lines 20-34).

15. As per claims 7-8, Dubey teaches that wherein said processor does not permit a store instruction in the pre-execution thread to modify main system memory contents (col. 15, lines 5-13; col. 40, lines 1-45).

16. As per claim 9, Dubey further teaches a buffer into which pre-execution thread stores data is written to make such store data available to pre-execution thread load instructions (col. 15, lines 59-64).

17. As per claim 10, it is rejected for the same reason as claim 1 above. In addition, Dubey teaches:

a fetch unit capable of fetching instructions from a plurality of threads (fig. 1A, item 115; col. 6, lines 20-28);

a program counter coupled to said fetch unit; an instruction cache coupled to said fetch unit (fig. 1A, item 120; col. 6, lines 29-51); and

a data cache coupled to said instruction cache (fig. 1A, item 110; col. 6, lines 13-19).

18. As per claims 11-18, they are rejected for the same reason as claims 2-9 above.

19. As per claim 19, Dubey teaches the invention as claim including a method of running a program in a processor comprising:

inserting pre-execution thread instructions in the program (abstract; fig. 2A; col. 44, lines 55-58);

spawning a pre-execution thread when designated by the inserted instructions (col. 21, line 12 through col. 22, line 15); and

running said pre-execution thread concurrently with a main thread wherein both the pre-execution and the main threads include instructions from the same program, the pre-execution thread running a head of the main thread and containing only a portion of the instructions from the main thread (abstract, lines 1-6; col. 4, lines 51-58; col. 6, lines 13-28; col. 7, lines 4-30; col. 8, lines 60-65; col. 15, line 45 through col. 16, line 13; col. 21, lines 25-38).

20. As per claims 20, 22-24, and 26-29, they are rejected for the same reason as claims 2-9 above.

21. As per claim 21, Dubey teaches copying register contents associated with the main thread to registers used by the pre-execution thread (col. 8, lines 3-18).

22. As per claim 25, Dubey teaches copying the contents of at least one register to memory to make such contents available to the pre-execution thread (col. 8, lines 3-18).

23. As per claim 30, Dubey teaches that wherein inserting pre-execution thread instructions in the program including inserting a stop instruction which causes the processor stop the pre-execution thread (abstract; fig. 2A; col. 44, lines 55-58).

24. As per claim 31, it is rejected for the same reason as claim 10 above. In addition, Dubey teaches that wherein, in a pre-execution thread, said processor pre-executes instructions from a main thread that are specified by said main thread (abstract, lines 1-6; col. 4, lines 51-58; col. 6, lines 13-28; col. 7, lines 4-30; col. 8, lines 60-65; col. 15, line 45 through col. 16, line 13; col. 21, lines 25-38).

25. As per claim 32, Dubey teaches that wherein a pre-execution thread is caused to be spawned to pre-execute said instructions by an instruction in the main thread

(abstract, lines 1-6; col. 4, lines 51-58; col. 6, lines 13-28; col. 7, lines 4-30; col. 8, lines 60-65; col. 15, line 45 through col. 16, line 13; col. 21, lines 25-38).

26. As per claim 33, Dubey teaches that wherein a pre-execution thread spins on a variable that is set to a predetermined value by the main thread when there are instructions to pre-execute (col. 18, lines 23-34).

27. As per claim 34, Dubey teaches that wherein the processor ceases pre-executing instructions when a program counter is encountered that exceeds a range (col. 9, lines 9-27).

28. As per claim 35, Dubey teaches that wherein the processor ceases pre-executing instructions when the main thread catches up to the pre-executing instructions (col. 13, lines 8-32).

29. As per claim 36, Dubey teaches that wherein the processor ceases pre-executing instructions when the number of pre-executing instructions exceeds a limit (col. 9, lines 9-27).

Response to Arguments

30. Applicant's arguments filed on 05/01/2006, with respect to the rejection(s) of claim(s) 1-36 have been fully considered and are persuasive. Therefore, the rejection

has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure are disclosed in PTO-892.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer N. To whose telephone number is (571) 272-7212. The examiner can normally be reached on M-T 6AM- 3:30 PM, F 6AM- 2:30 PM.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer N. To
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